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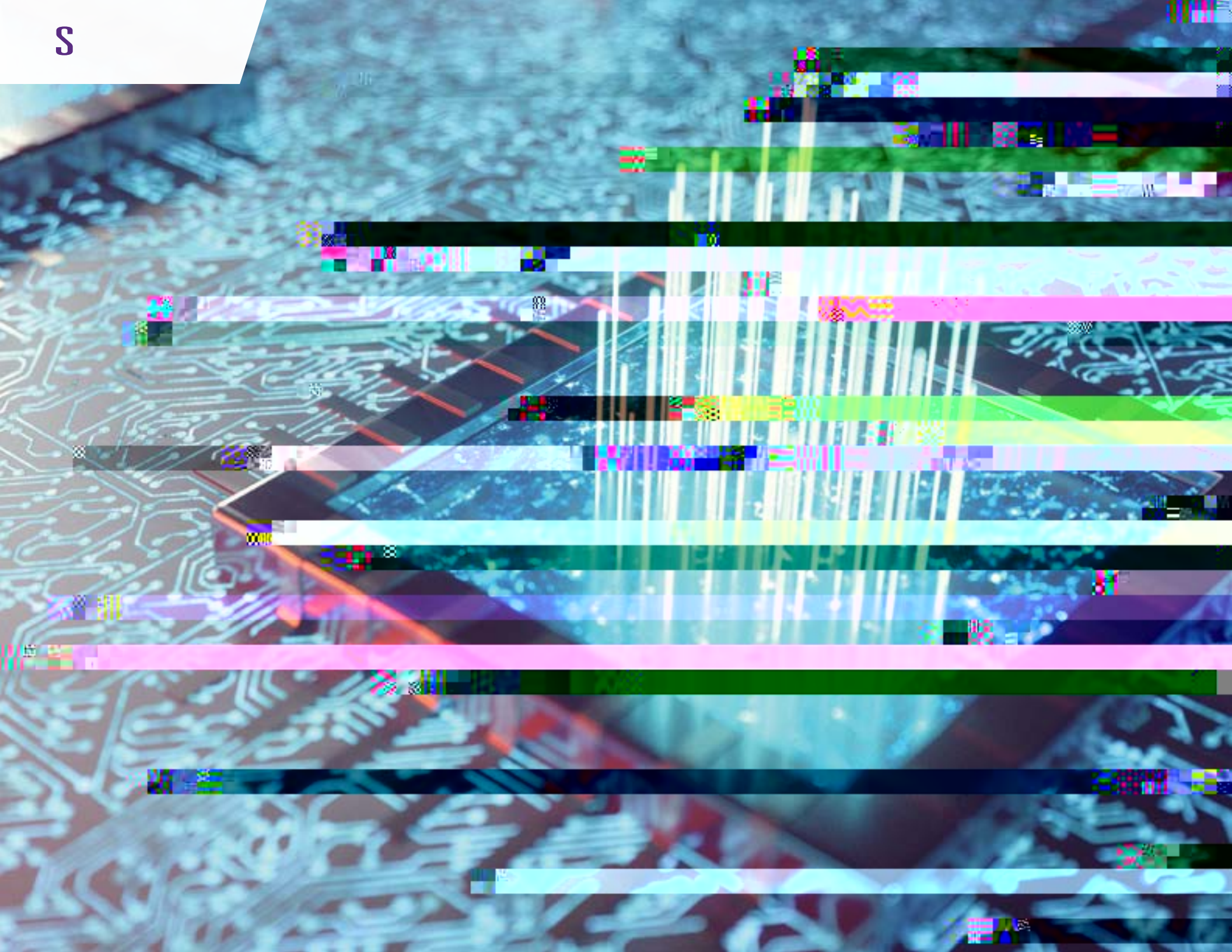


Broad IP Portfolio

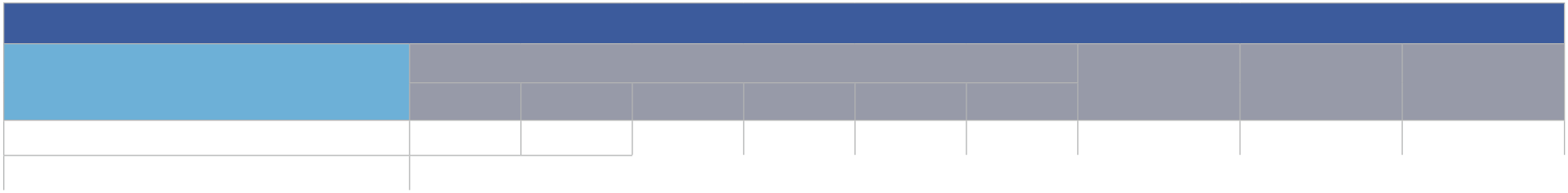
Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate IP integration, software development, and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, pre-verified and customizable IP subsystems, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

Interface IP													
Die-to-Die	Process Technologies							Controllers	Supported Protocol				Verification IP
	16nm	12nm	7nm	6nm	5nm	4nm	3nm		Streaming	CXS	CHI-C2C	CXL	
UCIe					✓	✓	✓	✓	✓	✓	✓	✓	✓
HBI/AIB	✓		✓		✓								
112G XSR		✓	✓	✓	✓			✓		✓			

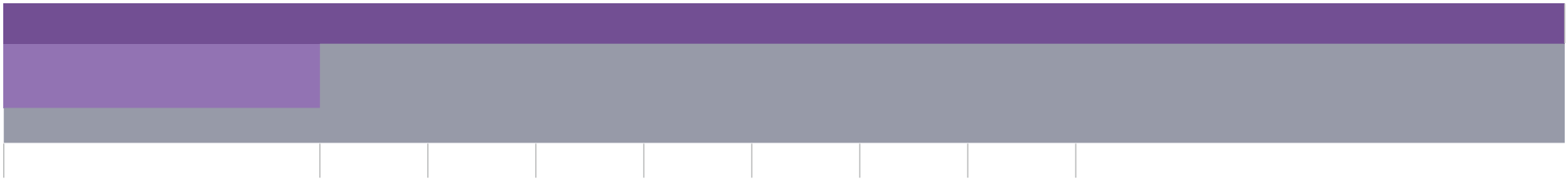
PCI Express	Process Technologies										Controllers	Configuration	IDE Security Module	HS Access & Test	Verification IP	Auto Grade
	40/45/55/65nm	28nm	22nm	20nm	12/14/16nm	8/10nm	7nm	5/6nm	3/4nm	2nm						
PCIe 6.x								✓	✓		Endpoint, Root Port, Dual Mode, Switch	x2, x4, x8, x16	✓	✓	✓	
PCIe 5.0					✓	✓	✓	✓	✓	✓	Endpoint, Root Port, Dual Mode, Switch, Embedded Endpoint	x1, x2, x4, x8, x16	✓	✓	✓	✓
PCIe 4.0		✓			✓		✓	✓	✓		Endpoint, Root Port, Dual Mode, Switch, Embedded Endpoint	x1, x2, x4, x8, x16	✓	✓	✓	✓
PCIe 3.1		✓	✓		✓	✓	✓	✓			Endpoint, Root Port, Dual Mode, Switch, Embedded Endpoint	x1, x2, x4, x8, x16	✓	✓	✓	✓
PCIe 2.1	✓	✓	✓	✓	✓		✓				Endpoint, Root Port, Dual Mode, Switch, Embedded Endpoint	x1, x2, x4, x8, x16		✓	✓	✓

Interface IP				
Bluetooth, Thread, Zigbee	Process Technologies		Controller (Link Layer / MAC)	BLE Host SW
	40nm	22nm		
Bluetooth 5.x RFPHY (Radio + Modem)	✓	✓		
Bluetooth LE 5.2 Link Layer Combo 15.4 MAC			✓	
Bluetooth LE 5.3 Link Layer Combo 15.4 MAC			✓	
Bluetooth LE 5.4 Link Layer Combo 15.4 MAC			✓	
IEEE 802.15.4 (Thread, Zigbee) MAC			✓	
				✓

AMBA	Synthesizable IP	Verification IP	Auto Grade
AMBA APB 3/4, AHB 2/5, AXI 3/4, ACE-Lite interconnect fabric, bridges, interconnect matrices and infrastructure IP	✓	✓	
AHB controller	✓	✓	



Foundation IP													
Non-Volatile Memory	**Process Technologies**											**Bit Counts**	**Endurance (Write Cycles)**
	150/ 180nm	**110nm**	**130nm**	**80/ 90nm**	**55/ 65nm**	**40nm**	**28nm**	**22nm**	**16nm**	**12nm**	**5nm**		
One-Time Programmable (OTP)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	16 bit to 1 Mbit	1 per instance
Multi-Time Programmable (MTP) Medium-Density	180nm											16 bit to 512 Kbit	Up to 1,000
MTP EEPROM	180nm		✓		✓	✓						128 bit to 8 Kbit	Up to 1,000,000
MTP ULP	✓											64 bit to 4 Kbit	Up to 100,000
Few-Time Programmable (FTP) Trim	✓	✓	✓									64 bit to 4 Kbit	Up to 1,000
Auto Grade OTP			✓					✓				Up to 1 Mbit	1 per instance
Automotive AEC-Q100 Compliant OTP	✓				✓	✓	✓		✓			Up to 1 Mbit	1 per instance
Automotive AEC-Q100 Compliant MTP	✓		✓									128 bit to 8 Kbit (Up to 256Kb for Medium Density)	Up to 10,000



Processor IP											
ARC-V (RISC-V) 64-bit Processors	**Multicore Support**	**L1 Cache (I & D)**	**L2 Cache (unified, per core)**	**L3 Cache (shared)**	**MMU**	**Hardware Virtualization**	**Floating Point**	**Real-time Trace Support**	**Vector Extensions (RVV)**	**Safety Compliant (ISO 26262)**	**Cybersecurity Compliant (ISO 21434)**
RPX-100/100V		Up to 64KUp to 6ion									

					MPU	MMU	Floating Point (SIMD)	Trace
HS66, HS66MP	Up to 12 (MP)	Up to 16M	Up to 64K	Up to 64M	Opt	Opt	Opt	Opt
HS68, HS68MP	Up to 12 (MP)	Up to 16M	Up to 64K	Up to 64M	Opt	✓	Opt	Opt

ARC VPX DSP Processors	Multicore configurations	Vector Execution Units/VLIW	Vector Length	Vector Floating Point Unit	Vector Math Accelerator (configuration option)	Safety Compliant (ISO 26262)
VPX2/VPX2FS	1, 2	3	128-bit	Opt	✓	✓ (FS only)
VPX3/VPX3FS	1, 2	3	256-bit	Opt	✓	✓ (FS only)
VPX5/VPX5FS	1, 2, 4	3	512-bit	Opt	✓	✓ (FS only)

ARC NPX Neural Processors	MACs	L2 Shared Memory	Tensor Accelerator	Tensor Floating Point Unit	Memory Management Unit (MMU)	Virtualization Support	Safety Compliant (ISO 26262)
NPX6-1K/NPX6-1KFS	1024	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-4K/NPX6-4KFS	4096	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-8K/NPX6-8KFS	8192	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-16K/NPX6-16KFS	16384	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-24K/NPX6-24KFS	24576	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-32K/NPX6-32KFS	32768	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-48K/NPX-48KFS	49152	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-64K/NPX6-64KFS	65536	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-96K/NPX6-96KFS	98304	0-64 MB	✓	Opt	✓	✓	✓ (FS only)

IP Accelerated Initiative

With IP Accelerated, Synopsys has augmented its broad portfolio of silicon-proven Synopsys IP portfolio with SoC architecture design support, IP subsystems, signal integrity/power integrity analysis and IP hardening, and comprehensive silicon bring-up support to accelerate your product development cycle.

IP Subsystems support many protocols and deliverables for IP integration including configuration scripts, test environment, test scripts, linting, CDC checks, RDC checks, synthesis scripts and implementation scripts. The subsystems also include AMBA or native bus, clock management, reset, DMA, interrupts, memory, power management, debug and test logic.

Hardening and SIPI provide a GDSII for integration in an SoC and include on-chip decoupling capacitance, power and ground pins, PHY and SDRAM termination strategy, SoC package design, PCB stack-up and trace width/spacing, performance at required data rate, read/write/address, and command/control timing budgets.

With your vision and our expertise, we can tune our IP to your SoC, enabling your team to focus on product differentiation.

IP Subsystems				
Interface IP Subsystems	**Supported IP**	**Multi-Protocol Support**	**Integrated Logic**	**Included Scripts**
	USB, PCIe, DDR, HBM, UCIe, Ethernet, MIPI, AMBA, Security, MACsec, PCIe switch, CXL 2.0 switch	✓	AMBA or native bus, clock management, reset, DMA, interrupts, memory, power management, debug and test logic	scripts, linting, CDC checks, RDC checks, synthesis scripts, implementation scripts

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