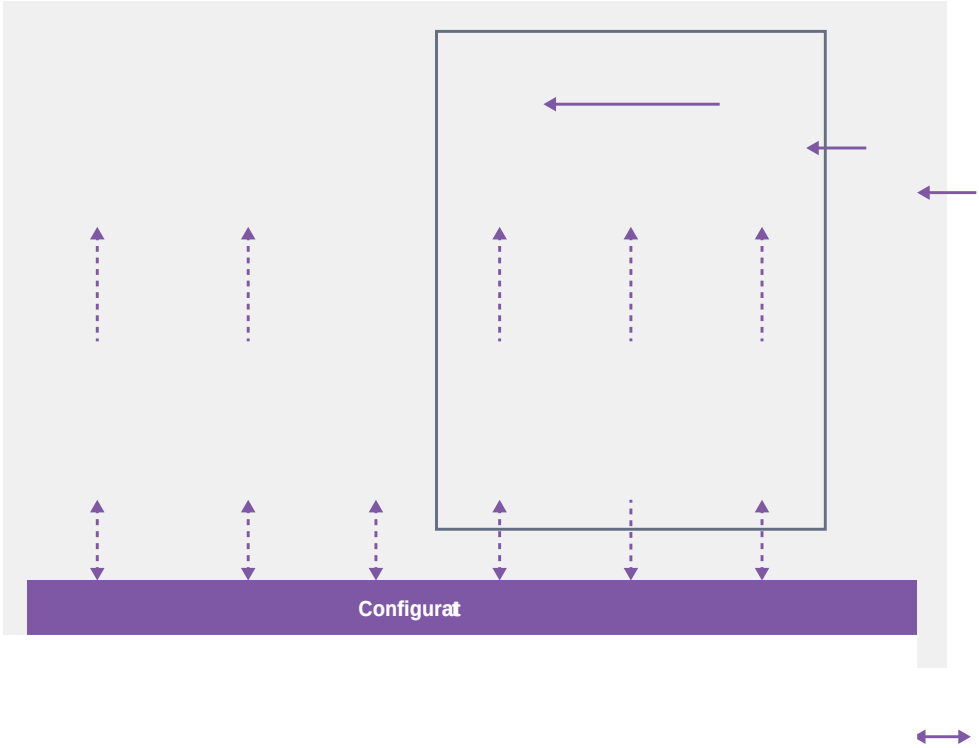
Overview

The Synopsys Ethernet 100G MAC IP, compliant with the IEEE802.3/802.3ba standard, implements the full MAC layer and reconciliation sub-layer for 10/20/40/50/100G operation. The IP also supports industry standard 25/50G operations.

Configuration pins are available to dynamically set the Synopsys IP to terminate and form MAC frames (NIC application) or to pass MAC frames to the application or the Ethernet line without modifications. In either application, the IP supports IEEE managed objects, IETF MIB-II and RMON.

On the application side, the MAC implements a flexible FIFO interface that can be connected to a custom user application. On the Ethernet line side, the MAC implements a wide CGMII/XLGMII (100G/40G Medium Independent Interface) for a 10G operation.

The IP supports Energy Efficient Ethernet (EEE) signaling for power management as per defined by the IEEE 802.3az standard.


Configurat

- Two classes of traffic classification for AVB applications in the preemptable MAC
- Optional Ethernet Pause Frame (802.3 Annex 31A) termination providing fully automated flow control without any user overhead
- supports optional Priority Flow Control (PFC) frame supporting 8 classes for higher layer congestion management and supports 16 classes via a synthesis parameter
- Optional 802.3 basic and mandatory managed objects statistic counters and IETF Management Information Database (MIB) package (RFC2665) and Remote Network Monitoring (RMON) counters

Deliverables

- SystemVerilog RTL Source code
- Verilog Testbench environment with example testcases
- Scripts and constraints files for implementation tools like Spyglass Lint/CDC, DesignCompiler, etc.
- IPXACT views for register maps
- Documentation: Databook, Integration User guide and Release Notes

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and otyping kitsl(subsystems)TjETEM

06/02/22.CS890319168-100G Ethernet MAC IP with TSN DS.