Synopsys and Socionext

Ensuring Testability of an Ultra Large Scale HBM-Based Multi-Die SoC for AI and HPC

“Multiple design groups from Socionext and Synopsys collaborated as a cross-functional team to satisfy the design for test (DFT) requirements on a challenging multi-die system-on-chip (SoC) project with a master die chiplet and four High Bandwidth Memory (HBM) modules. We completed all DFT items and successfully shipped the product on schedule, at the target data rate, and without any impact on logic die size.”

~Shinichiro Ikeda, Senior Principal Engineer, Socionext Inc.

Challenges

The trends driving ultra large scale system-on-chip (SoC) designs include advanced applications such as artificial intelligence (AI) and high performance computing (HPC) with the need for multi-terabyte/second memory bandwidth. To satisfy these needs, die-to-die (D2D) chiplet technology is required to connect these SoCs with High Bandwidth Memory (HBM). To satisfy these demands, Socionext developed a 2.5D chiplet-based SoC containing a master die and four HBM modules. Such a device could not be tested in production using conventional single-die methods, so a comprehensive design for excellence (DFX) strategy was required.

Project Overview

The Socionext ultra large scale SoC is shown in Figure 1. There are 1700 High Bandwidth Interconnect (HBI) signal connections between the master die and each HBM module, for a total of 6800 within the multi-die package. None of these are accessible on production automatic test equipment (ATE), one of the reasons that an innovative DFX approach was needed. Design for test (DFT) had to support test and analysis of the HBM as well as test, analysis, and repair of the HBI. The overall package was 4.225mm2 (65mm by 65mm) in size, with a total of 4,040 solder balls in a ball grid array (BGA) configuration.

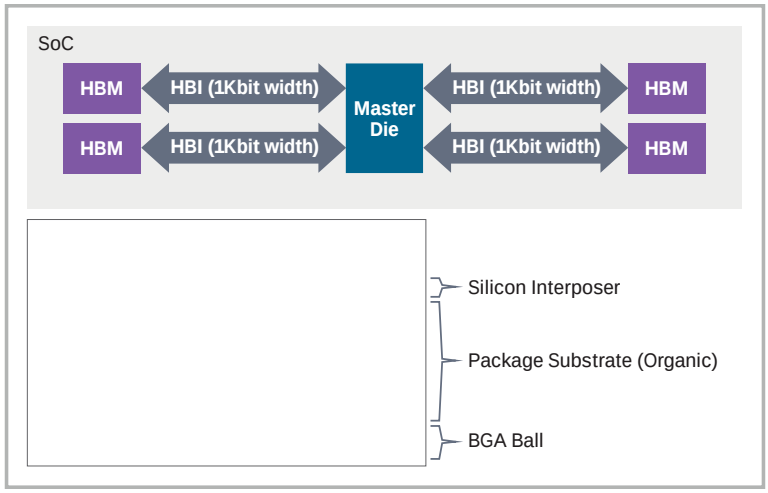

Figure 1: Overview of the Socionext multi-die design

The Synopsys Solution

Multiple design groups from Socionext and Synopsys formed a single cross-functional team to codify the DFX requirements and identify a solution. The experts on this team had a broad range of knowledge, including HBM DFT requirements, HBM PHY IP, electronic design automation (EDA) DFT tools, multi-die packaging, and production manufacturing. Their solution started with the selection of SLM IP from Synopsys to satisfy overall DFX requirements without any impact on memory bandwidth or die size. For the master die, the team chose the Synopsys HBM PHY IP as well as the following IP:

- Synopsys SLM SHS IP, an automated hierarchical test solution for efficiently testing SoCs with multiple analog/mixed-signal, digital logic, and interface IP by creating a hierarchical IEEE 1500 network with pre-validated production ready ATE patterns with automated pattern porting
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