High-Speed Access & Test

For Test and In-field

Overview

SiliconMAX™ High-Speed Access and Test (HSAT) IP combined with Synopsys TestMAX ALE software uses standard high speed IO interfaces such as PCIe and USB, to get test, debug and monitoring data in and out of an SoC at Gigabit data rates and avoids the need for large numbers of test and interface pins. Test time can be reduced because the link between the test time and GPIO data rate is eliminated. Further, this solution provides a key component for SiliconMAX Silicon Lifecycle Management platform allowing manufacturing tests to be repeated in-system and in-field as well as providing high speed access to PVT and functional monitor data.

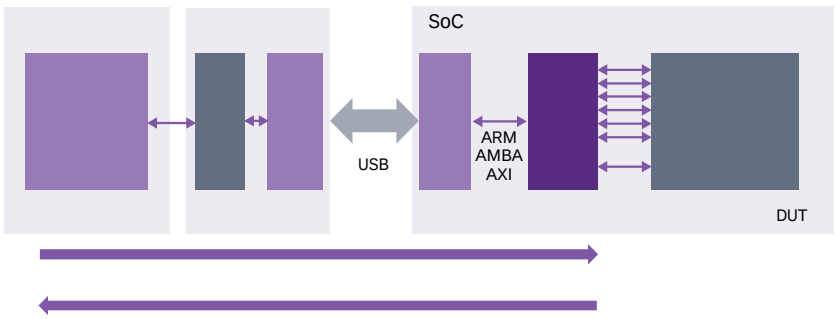

Figure 1: SiliconMAX High-Speed Access and Test IP and Synopsys TestMAX ALE Solution

Highlights

- Reuse HSIO interfaces (PCIe and USB) for test and other data avoiding the need for very large numbers of test pins
- Speed up test by exceeding GPIO test pin data rates
- Easily repeat manufacturing tests in-system and in-field
- Enhance testing in-system and in-field with updated tests
- High speed access to PVT monitors, debug and other sensor data
- Bandwidth scales with each new generation of HSIO (PCIe, USB)

Target Applications

- Large SoCs with high test volume and pin limitations
- Applications where in-field reliability is key
- High performance compute, AI and server
- Desktops, notebooks and workstations
- Industrial, automotive and IoT
- Smartphones and 5G Infrastructure

Key Features

- PCIe, USB high speed IO for ATE, in-system and in-field
- Can use other available interfaces (e.g. SPI) for in-system/in-field
- Configurable Arm® AMBA® AXI slave interface to HSIO
- Configurable number of scan chains (512 max) and TAP port supported
- Full RTL configuration and integration flow
- Arm AMBA AXI testbench generation
- Optional EBC interface for USB
- Bypass mode allows scan chains to connect to HS Access or GPIO pins
- Multiple levels of loop back for link validation

Key Benefits

- Reduce test time by eliminating the constraint of GPIO test pin data rate
- Re-use of HSIO pins (PCIe and USB) for test and other data