SY OPS S

SLM Clock & Delay Monitor IP

2 F I F S I L T F NLSF

Highlights

& F I F R F R S
S T I L

T MNLM U I MNLMF F S
T P V N I

1T T MFI T I F F U T NSL

8R F T R F T

)& NS L F NTS T F TR F I NS NTS
FSI TSS NTS

(FU F T NNTSU N F FS
FL T N N

Use Cases

(T P NS NTSI F

(T PI

2 R T F NR

) F NS MFF N N

7NSL T NF T V S

Overview

8 STU 812 (T P) F 2 TSNT ( ) 2 .5 N F R F UN T .5
MNM FS NS I NS NNTS NMT R MF F T MFI . I T S
S I FS F F MNLM U I S T PFSI U T N F F NR
I F R F R S . FS I T R F NSL T PI R R T
F NR I F NS MFF N N . MF . NS F T
TSS NSL T F N M 812 ( ) 2 .5 N F TF FNF F FS.8
&8.1 FI U TI

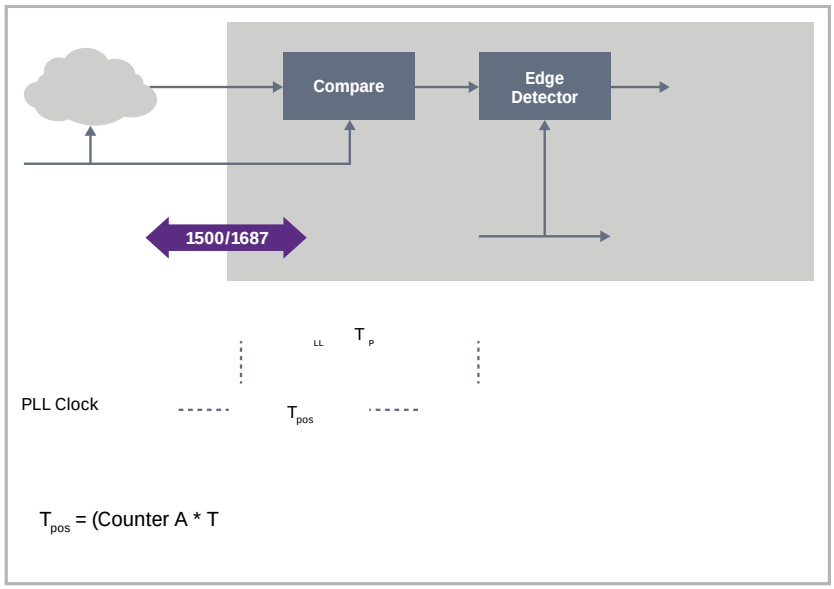

Figure 1: Synopsys SLM Clock & Delay Monitor IP

SLM Functional Monitors

S NTSF R TSNT F P T M T 8NNTS 1N 2 FSFL R S
812 M R TSNT F R II I NS M NNTS FSI UT T M F MT
NNF S NTS T M MNU) F F TR S NTSF R TSNT FS T I
F FS FL T NNTS N FSI FSF I TLF M NS NLM F I TS
M NS NLM F NTS FS FP S T NR U T U T R FS T R NNLF FS
TU F NTSF N 2 R T (5 T P TFI NS F T P I F F TR
NNF S NTS TSF 8 (T MR TSNT NSL 8 STU S NTSF R TSNT F
SF I NM)& FSI T F F TR F NTS T F T

Key Features

T MLM U I MLMF F S T P V N I
8R F TT U NS
& FNF F T .5 NM NNN T TR N

Key Benefits

(T PI V F N M P
2 R T F NR F PNSL NM .8
) NLNF I F NS MF F NF NTS
U NR N NNTSU T R FS T F NNF FUUNF NTS

Complete solution in SHS/SMS environment for Memory Read Time

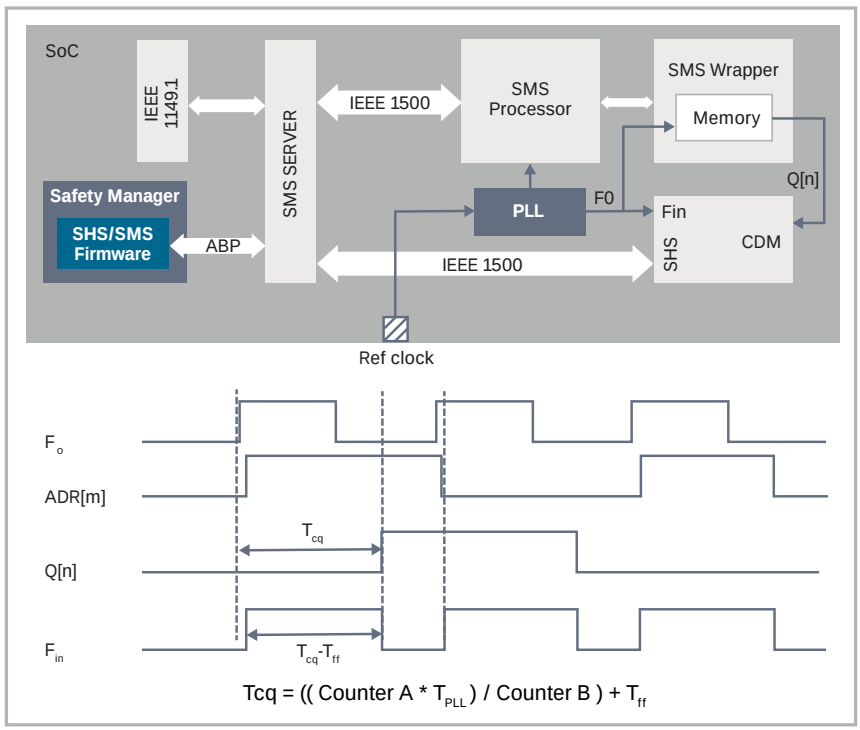

Figure 2: SHS/SMS based solution

About Synopsys IP

8 STU NF FI NSL UT N T MLMV F N NNTSU T S.5 T NTS T 8T(I NLS M TFI 8 STU .5 UT TNT NS I TLN N F N R II I R RT N 5 S T R II I FSFSTLF.5N

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