## **Synopsys**°

a II 2

#### SYNOPSYS IP DATASHEET

# Memory output data CDM IP Data input Pulse gen Counter A Asynchronous

#### **Key Features**

- No high-speed high accuracy reference clock required
- Small footprint
- Available as soft IP with flexibility to customize

### Key Benefits

- Clock duty cycle quality check
- Memory access time tracking with BIST
- Digital delay line test characterization
- Optimize silicon performance for safety critical applications

#### Complete solution in SHS/SMS environment for Memory Read Time



