Clock Jitter Analysis
with femto-second resolution

presented by:

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The analysis of clock jitter has evolved as data rates have increased. In high speed serial data links clock jitter affects data jitter at the transmitter, in the transmission line, and at the receiver.

Measurements of clock quality assurance have also evolved. The emphasis is now on directly relating clock performance to system performance in terms of the Bit Error Ratio.

Agenda

- Jitter in serial data applications
- The role of reference clocks in serial data applications
- Reference clocks and phase noise
- Reference clock quality analysis
- The toolset

In this seminar we concentrate on clock-jitter issues relevant to serial data systems.

After an introduction to the problems that jitter causes in serial data applications, the role of reference clocks and how their jitter affects the rest of a system is covered.

With the context and issues of reference clocks in place, a review of phase noise sets the stage for the discussion of techniques for evaluating clock quality with emphasis on emerging techniques for compliance testing.

We conclude with a survey of jitter analysis equipment.

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- **The role of reference clocks in serial data applications**
- **Reference clocks and phase noise**
- **Reference clock quality analysis**
- **The toolset**

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Introduction to jitter

Why do we care about jitter?

- Just as a low signal-to-noise ratio causes errors when the signal fluctuates *vertically* across the sampling point…
- Jitter causes errors when the signal fluctuates *horizontally* across the sampling point
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Jitter caused by phase noise

Consider a clock signal

ideal: $v_{ideal}(t) = v_0 \sin\omega t$

real: $v_{real}(t) = (v_0 + \Delta v(t)) \sin(\omega t + \varphi(t))$

Phase noise term, $\varphi(t)$ shifts the signal horizontally.

phase noise is the primary cause of jitter in clocks

Amplitude noise can also cause jitter..

Clock jitter is dominated by phase noise.

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The characteristics of jitter

The characteristics of jitter

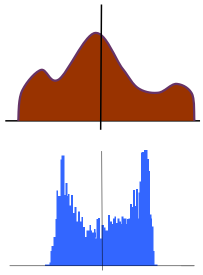
Deterministic Jitter – DJ

– Effects of a few processes

Electromagnetic interference $*$ reflections $*$ channel frequency response

Combines to form bounded distributions of varying shapes

$$DJ = \mathbf{DJ(p\text{-}p)}$$



The **net jitter PDF** is the convolution of RJ and DJ:

$$\boldsymbol{J} = RJ * DJ$$

Therefore, the jitter PDF is unbounded.

peak-to-peak jitter is not well defined!

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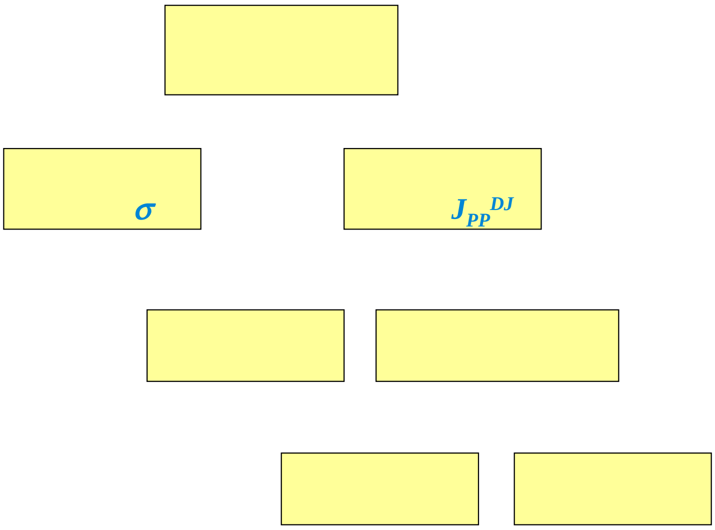
DJ is caused by a comparatively small number of processes that need not be independent and may have large magnitude.

It is called “deterministic” jitter because, in principle, if we knew everything there is to know about a system, we could accurately predict the jitter of each edge.

<u>The important thing about DJ is that its PDF is bounded.</u> Hence, unlike RJ, DJ has a well defined peak-to-peak value, DJ(p-p).

<u>The (actual or net) jitter PDF is the convolution of RJ and DJ and, due to the RJ component, it is unbounded.</u> Because it is unbounded, the peak-to-peak value of the jitter PDF is not well defined. In fact, the longer it is measured, the larger it is likely to become.

Jitter categories



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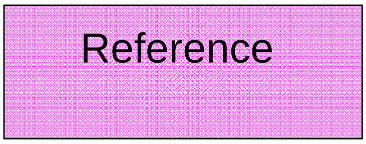
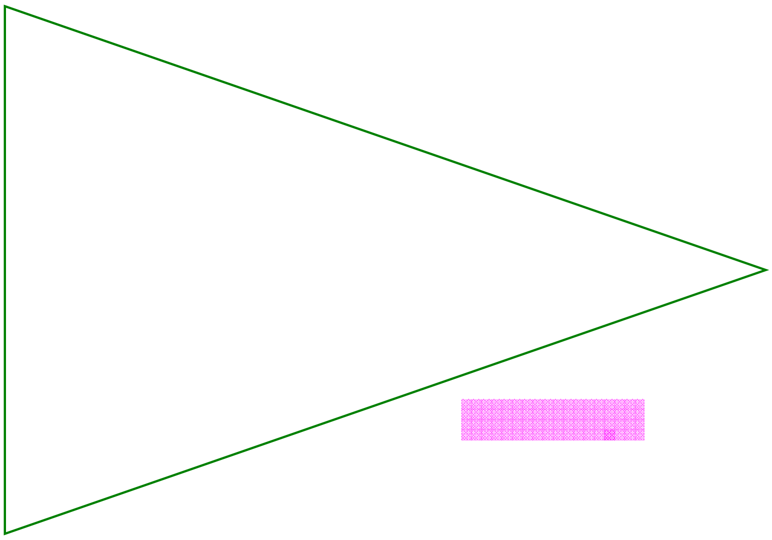
The role of the reference clock



Effect of clock jitter in a transmitter (1)



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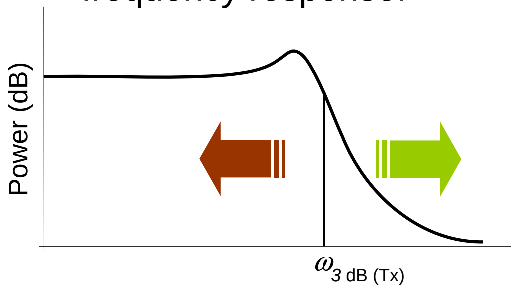
Effect of clock jitter in a transmitter (2)

The PLL multiplier has three important characteristics

1. The multiplying act amplifies the clock jitter.
2. Its VCO introduces more RJ and nonlinearities in its circuitry can introduce more DCD.
3. **There is a bandwidth associated with the PLL.**

Typical 2nd order PLL frequency response:



What clock jitter matters?

The PLL multiplier in the transmitter has a certain frequency response [i], typically a second order response like the one shown.

The non-uniform frequency response raises an interesting question:

What clock-jitter actually matters?

If the PLL were perfect and had zero bandwidth, then it would filter out all the clock-jitter and provide the transmitter with a jitter-free time-base.

Of course, zero bandwidth means infinite lock time, so we have to compromise, but the narrower the PLL bandwidth, the less jitter from the reference clock makes it into the data.

Determining whether or not a clock will function in a system at the desired BER requires careful testing of the jitter frequency spectrum.

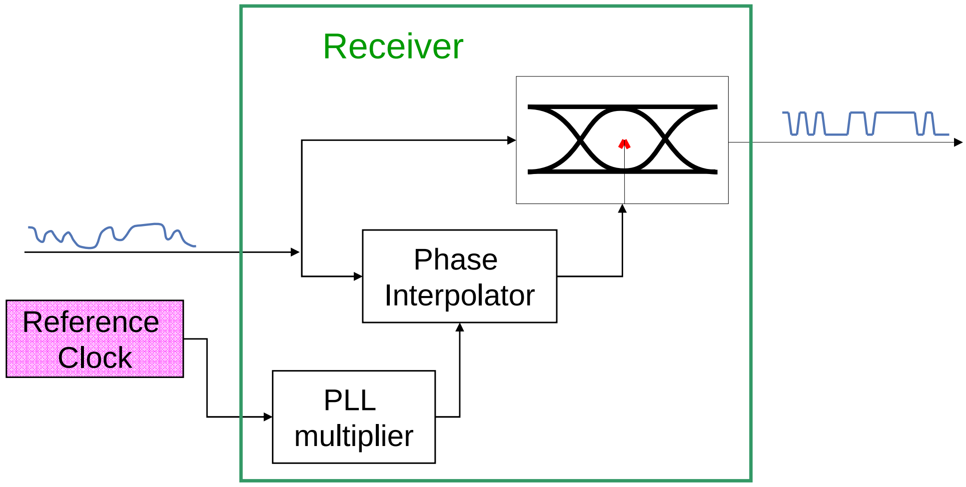
[i] F.M. Gardner, *Phaselock Techniques 3rd Edition*, New York: Wiley & Sons, 2005; Dan Wolaver, *Phase-locked Loop Circuit Design*, Prentice-Hall, 1991.

Role of the clock in a receiver (1)

The PLL recovers a f_d clock from the data

Defines the sampling point

Role of the clock in a receiver (2)



.. then how do you analyze clock jitter ?

1. Determine the limiting requirements of the specific system.
   e.g., PCI-Express, FBD, sATA, Fiber-Channel, ..
2. Apply the limiting case transmitter and receiver transfer

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- **Reference clocks and phase noise**
- Reference clock quality analysis
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We discuss the SSB spectrum, how to distinguish phase noise from amplitude noise, and, once again, the relationship of phase noise and jitter in this section.

Oscillator noise

An ideal oscillator: $v_{ideal}(t) = v_0 \sin 2\pi f_c t$

A real oscillator: $v_{real}(t) = (v_0 + \Delta v(t)) \sin(2\pi f_c t + \varphi(t))$

- **Sources of Noise**
  - Temperature, pressure, humidity – change frequency
  - Vibration – causes spurs
  - Electromagnetic fields – change the frequency, can cause spurs
- **Properties of Noise**
  - Phase noise cannot be eliminated by a limiter.
  - Noise close to the carrier cannot be eliminated by filtering.

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At frequencies closest to the carrier, the primary noise source is the non-zero width of the resonance. A noiseless oscillator would have zero bandwidth and infinite quality which, not coincidentally, implies zero resistance and can only be achieved in superconductors [i]. Far from the carrier, the usual suspects such as power supply feed-through, impedance mismatches, and so forth from the oscillator feedback loop affect both the phase and amplitude of the oscillator [ii].

Thermal noise, such as Johnson noise, causes white noise. Temperature and pressure affect the crystal geometry and, consequently, its resonant frequency. Spurious frequencies can be generated, typically tens of kHz above the desired resonance, by vibration of the crystal. In the frequency domain, the spurious frequencies appear at integer multiples of the difference of the vibration and carrier frequencies.

There are two significant practical system level problems caused by oscillator noise.

First, the power of the noise is taken from the carrier.

Second, as described above, when the oscillator frequency is multiplied up to the data rate, the resulting phase noise is increased by the square of the multiplication factor. That is, the sidebands increase 20 dB for every factor of ten in the multiplier.

Unfortunately phase noise can not be eliminated by a limiting-amplifier and, since so much of the noise is close to the carrier, it can not be eliminated by filtering.

[i] Alan M. Kadin, *Introduction to Superconducting Circuits*, Wiley-Interscience, 1999.

[ii] Burkhard Schiek, Heinz-Juergen Siweris, Ilona Rolfes, *Noise in High-Frequency Circuits and Oscillators*, Wiley-Interscience, 2006.

Clock signal

Phase noise in the frequency domain

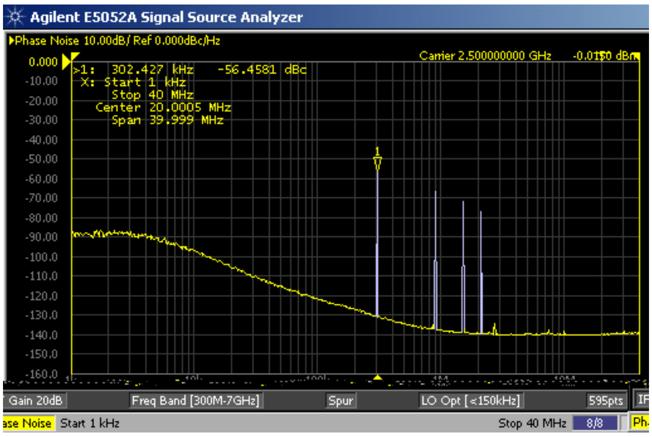
$$S_\varphi(f_\varphi) = \left|F[\varphi(t)]\right|^2 = \left|\tilde{\varphi}(f_\varphi)\right|^2$$

Phase noise analyzer plots the

Phase Spectral Density, $S_\varphi(f_\varphi)$

The phase noise frequency domain is given by the **offset frequency**,

$$f_\varphi = f - f_c$$



$$\varphi \quad \varphi \quad \frac{\varphi ff \quad \varphi}{S \quad \varphi} \left[\mathrm{rad}^2/\mathrm{Hz}\right]$$

The SSB spectrum and the phase spectral density

$$L(f) = \frac{1}{2P_C}\frac{\Delta P(f_\varphi)}{\Delta f_\varphi}$$

$$= \frac{1}{\Delta f_\varphi}\frac{\frac{1}{2}\Delta v^2_{Noise\ rms}/R}{v^2_{Carrier}/R}$$

$$= \frac{1}{2\Delta f_\varphi}\frac{\Delta v^2_{Noise\ rms}}{v^2_{Carrier}}$$

$$= \frac{\Delta v^2_{rms}}{2\Delta f} = \tfrac{1}{2}S_v(f) \approx \frac{\Delta\varphi^2_{rms}}{2\Delta f_\varphi} = \tfrac{1}{2}S_\varphi(f_\varphi)$$

Δv_{noise}

$$\boxed{L(f)\left[{}^{\mathrm{dBc}}\!/\!{}_{\mathrm{Hz}}\right] = \tfrac{1}{2}S_V(f)\left[{}^{\mathrm{dBc}}\!/\!{}_{\mathrm{Hz}}\right] \approx \tfrac{1}{2}S_\varphi(f_\varphi)\left[{}^{\mathrm{rad}^2}\!/\!{}_{\mathrm{Hz}}\right]}$$

(if $|\Delta\varphi|$ is small enough.)

Phase noise and jitter

- Clock signal: $v(t) = (v_0 + \Delta v(t)) \sin(2\pi f t + \varphi(t))$
- Jitter is "the short term phase variation of the significant instants of a digital signal from their ideal

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There is significant historical momentum behind how clocks are evaluated. Many of the established techniques, like phase noise analysis, provide a solid foundation for clock quality analysis in high rate serial data systems.

Reference clock quality analysis

- Traditional clock specifications

  Phase, period, cycle-to-cycle jitter

  .. do not answer the fundamental question:

  Will the clock work in the system?

  – Only care about jitter that can cause errors
  – Need to analyze clock-jitter under application-specific specifications
    - Transmitter: multiplier bandwidth
    - Receiver: clock recovery bandwidth
- How do we read a clock data sheet?

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The quality of a clock depends on the point of view.

Traditional clock specifications like peak-to-peak phase jitter, period jitter,

Quantities quoted on clock data sheets

	Quantity	Some Typical Values (varies by application)
•	Cycle-to-cycle Jitter	30 ~ 150 ps
•	Phase jitter	30 ~ 80 ps
•	Peak-to-peak jitter (Without specifying number of cycles measured)	20 ~ 50 ps
•	rms of whole jitter distribution	2 ~ 5 ps
•	rms random phase jitter in named bandwidths	0.3 ~ 4 ps
•	Phase noise relative to carrier (at named offset frequencies) ofc0 gf41 T-8w 8Bc/Hz	~ 50 ps

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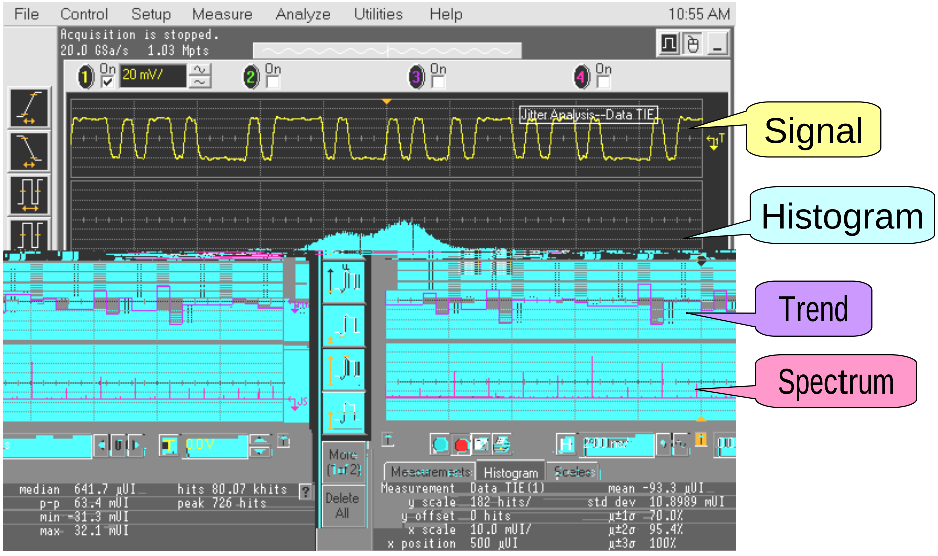
TIE analysis on a real-time oscilloscope

TIE



(TIE: Time Interval Error)

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Real-time oscilloscopes are the best tool for assembling the Time Interval Error (TIE) data set. First a signal is captured, the top trace in the above diagram, then the values of that signal at the voltage slice level are assembled giving the TIE data, { t_n }.

The actual data is acquired by extremely fast ADCs and so is not a truly analog trace. The precise crossing times must be interpolated from each set of two data points that bracket the slice level.

If the bandwidth of the oscilloscope is sufficient (three times the data rate is usually adequate) the interpolation should not introduce appreciable uncertainty.

With the TIE data in hand, the phase jitter histogram is easy to extract – a measure of the PDF – and the jitter trend, $\varphi(t_n)$ can be plotted.

Notice the distinction between the discrete jitter trend, $\varphi(t_n)$, and the continuous time-domain representation of the phase noise $\varphi(t)$. The jitter spectrum can be calculated by using the usual trick of padding the discrete data set, { t_n }, with zeros and applying a discrete Fourier transform [i].

Again, notice the distinction between the jitter spectrum, which is the Fourier transform of the crossing times and the phase noise spectrum which is the Fourier transform of the phase noise.

[i] William H. Press, et al., *Numerical Recipes in C++ The Art of Scientific Computing*, Cambridge University Press, 2002.

Jitter analysis on a Time Interval Error data set

TIE

Accumulate the crossing-point times, $\{\ t(n)\ \}$, on a real-time oscilloscope, then…

Measure peak-to-peak or rms phase, period, cycle-to-cycle jitter:

$$\Delta t_{phase}(n) = t(n) - nT$$

Determine max or rms $[\Delta t_{phase}(n)]$

$$\Delta t_{period}(n) = [t(n) - nT] - [t(n\text{-}1) - (n\text{-}1)T] = t(n) - t(n\text{-}1) - T$$

Determine max or rms $[\Delta t_{period}(n)]$

$$\Delta t_{cyc\text{-}cyc}(n) = [t(n+1) - t(n)] - [t(n) - t(n\text{-}1)]$$

Determine max or rms $[\Delta t_{cyc\text{-}cyc}(n)]$

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The TIE data set can be used to extract all of the phase, period, and cycle-to-

Time Interval Error analysis

TIE

Model the performance of a clock in a system with TIE data

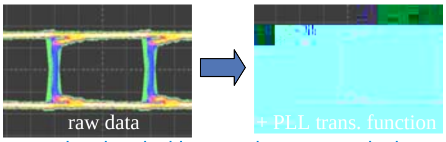
– Recall the second order PLL transfer function

$$H(s) = \frac{2s\zeta\omega_n + \omega_n^2}{s^2 + 2s\zeta\omega_n + \omega_n^2} \qquad \omega_{3\mathrm{dB}} = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{(1+2\zeta^2)^2 + 1}}$$

– Use DSP techniques to apply $H(s)$ to the data
  clock performance in the system!
  RJ,. DJ, and TJ(BER) contributions of the clock

Details.. The oscilloscope must have

– Sufficient Bandwidth to represent the signal frequency components
– Memory depth to acquire enough data that the DSP techniques are accurate
– Low noise



example: signal with spread spectrum clock

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The power of the TIE data in jitter analysis is tremendous.

Given the worst case transfer characteristics of the transmitter and receiver, the techniques of Digital Signal Processing [i] (DSP) can be used with impunity.

For example, the second-order PLL transfer function can be applied to the TIE data to determine the RJ and DJ that the clock will contribute to the TJ(BER) of the system.

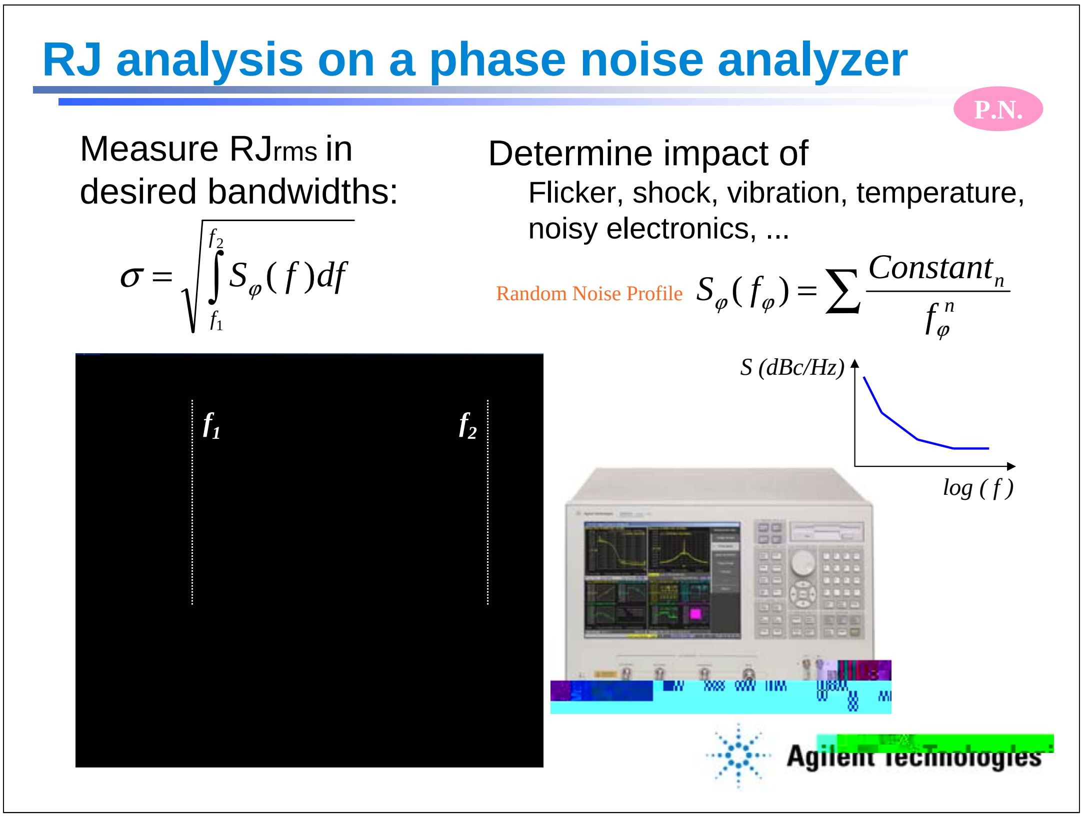
In practice, the TIE data must be provided by an oscilloscope with sufficient bandwidth to represent the signal and sufficient memory depth to provide enough data to assure accuracy.

The biggest drawback to use of TIE techniques is the signal integrity of real-time oscilloscopes.

While they are without question the most flexible tool in your lab, they can rarely compete with the fidelity of an equivalent-time sampling oscilloscope and can not approach the sensitivity of a phase noise analyzer.

[i] Emmanuel Ifeachor and Barrie Jervis, *Digital Signal Processing: A Practical Approach*, Addison-Wesley, 1993.

Phase Noise Analysis



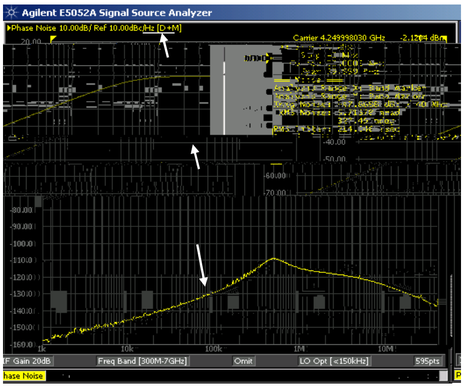
Two important goals can be achieved by analyzing RJ on a phase noise analyzer.

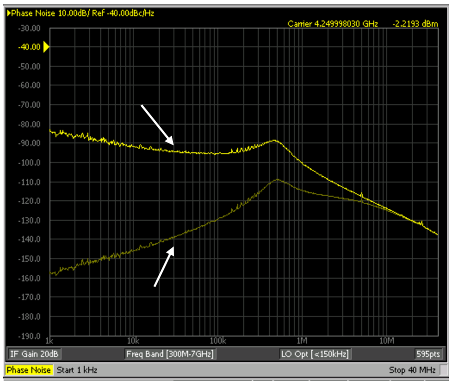
First, by integrating the RJ spectrum, the width of the corresponding RJ Gaussian distribution is extracted within the bandwidth of interest.

Second, the major causes of RJ can be isolated by analyzing the power-series behavior of $S\varphi(f\varphi)$.

Emulate jitter transfer function

P.N.





If H(s) is a PLL transfer function (of a receiver or clock recovery circuits), then 1-H(s) is a jitter transfer function, JTF.
In the offset frequency domain, it is very easy to emulate a specific JTF by filtering measured phase noise (spectral density) in a real time mode.

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This is an illustration of the effect of a PLL response function applied directly to the phase noise signal, $\varphi(t)$.

The jitter transfer function is what is left over after the clock recovery response is applied.

If <u>*H*(*s*)</u> is the clock recovery transfer function, then <u>1 - *H*(*s*)</u> is the jitter transfer function.

By applying the jitter transfer function to the phase noise spectrum, we are left with just that phase noise which can affect the system.

You can see how the low frequency jitter is suppressed.

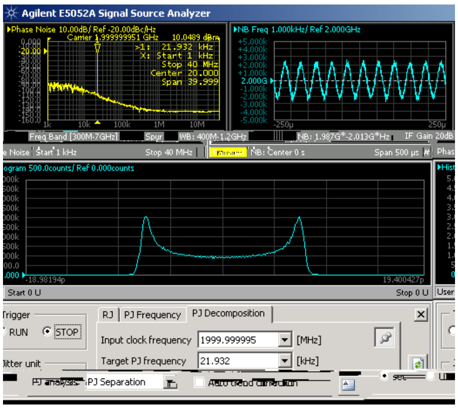
The ability to analyze just that phase noise which can affect the BER is a powerful tool.

PJ on a phase noise analyzer

P.N.

In the offset-frequency domain:

In the time domain:



$S_{\varphi}(f)$

$\varphi(t)$

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PJ causes sharp spurs in the phase noise spectrum.

Knowledge of the PJ frequencies is a terrific tool for diagnosing problems.

The time domain view shows how the combination of RJ and PJ smear the crossing point and cause errors.

It also allows extraction of the clock DJ which is required for compliance by some specifications.

The tools for clock-jitter analysis

Phase noise analyzers – SSA (Signal Source Analyzer)

- Agilent E5052B Signal Source Analyzer with precision clock jitter analysis software, E5001A (SSA-J)

Real-time oscilloscopes

- Agilent 80000 Series Infiniium oscilloscopes with E2688A Serial Data Analysis and EZJIT+ software

Equivalent-time sampling oscilloscopes – DCA

- Agilent 86100C Digital Communications Analyzer, DCA-J

Spectrum Analyzer – PSA

- Agilent E4440 series Performance Spectrum Analyzers, PSA

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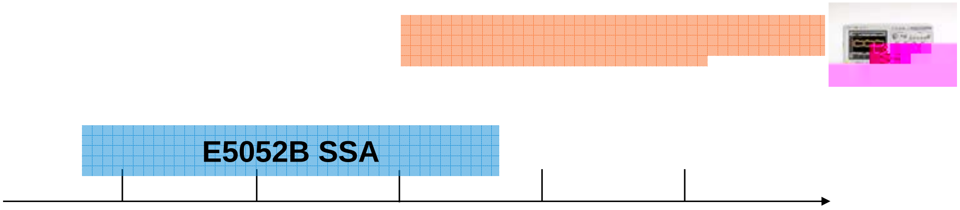
Capabilities of different clock jitter analysis equipment

Range for jitter measurements by different types of equipment



[redacted]

Fundamental differences

<u>Noise floor</u>

SSA ~ 10 fs <
equiv-time scope ~ 300 fs <
real-time scope ~ 2 ps

<u>Dynamic range</u>

SSA ~ multi-mUI
equiv-time scope ~ 1/4 UI >
real-time scope ~ multi-UI

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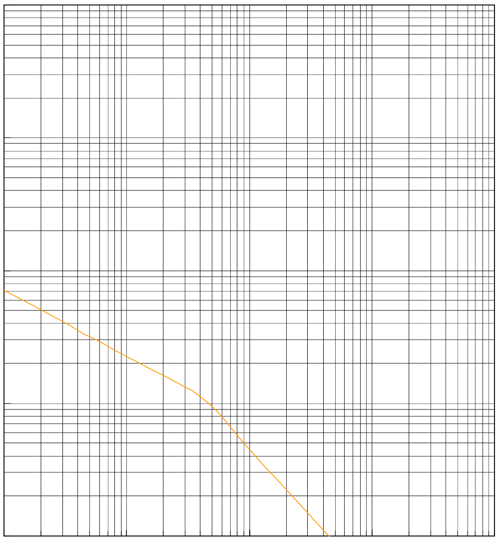
jitter noise floor [fs rms]



Conclusion

The goal is to

Determine the effect of Clock jitter on the BER of a system

* Clock-jitter is amplified by the transmitter multiplier,
* Has a frequency-dependent response to Clock Recovery.

If the jitter on the data is the same as the jitter of the sampling point no errors!

Small bandwidth on Transmitter PLL limits data-jitter.

Large bandwidth on Receiver Clock Recovery limits affect of jitter on BER.

>> Appropriate response (transfer function) models are necessary

Conclusion

Clock jitter analysis tool

Sub-pico-second accuracy and femto-second resolution with appropriate response (transfer function) models in clock jitter measurement is desired for recent high-speed data communication systems.

Phase noise analysis is one of the best promising ways to take, for accurate clock jitter measurement.

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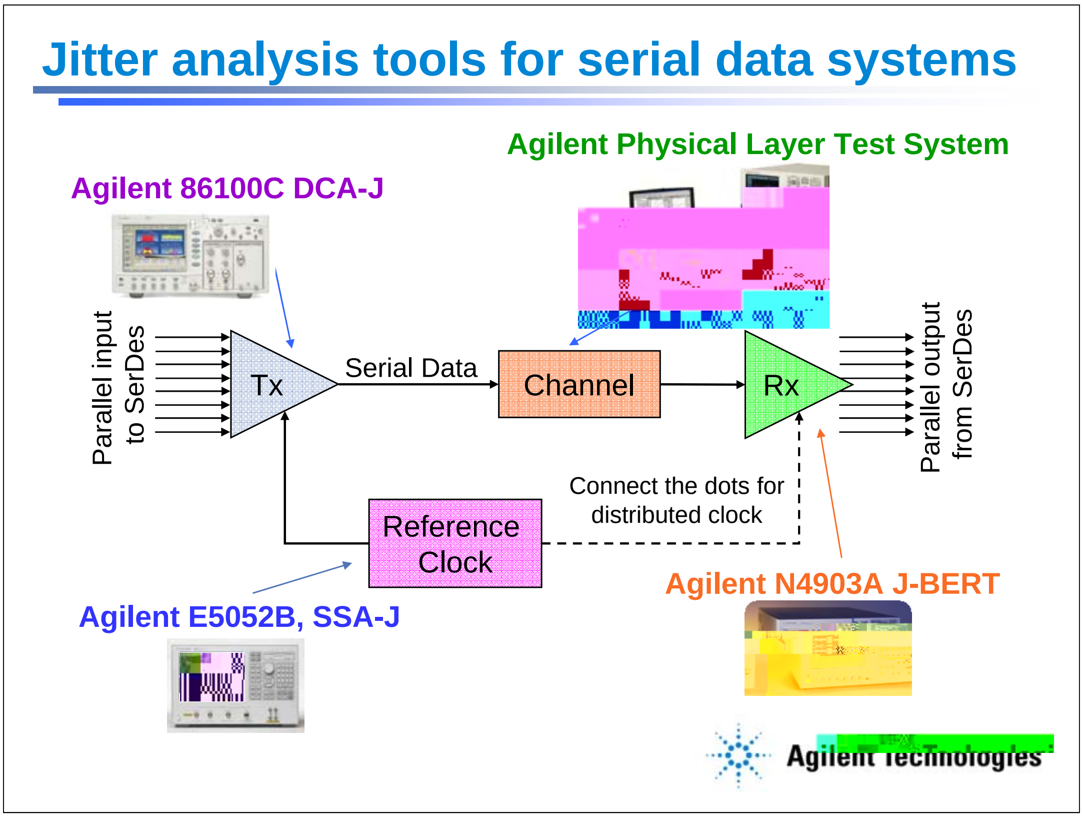

Agilent Technologies provides an exhaustive set of tools for jitter analysis on serial data systems.

Q & A

Q&A

- What clock frequency can the SSA measure?
  10MHz to 7GHz (E5052B) or 26.5GHz (E5052B+E5053A)
- What is SSA's jitter frequency bandwidth?
  100MHz
- How can I emulate jitter transfer functions with the SSA?
  Special utility software is available. Contact Agilent Sales.
- Can the SSA measure DCD (Duty Cycle Distortion)?
  No.
- Can the phase noise analysis measure cycle-to-cycle jitter?
  No.
- How can I find out more about the SSA and SSA-J?
  Refer to: www.agilent.com/find/ssa
  www.agilent.com/find/ssaj

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